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Design of Testable Reversible ALU using QCA Multiplexers

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Abstract: International Technology Roadmap for Semiconductors (ITRS) has indicated several new technologies alternative for CMOS nanotechnology, some of these include Resonant Tunneling Diodes (RTDs), Single Electron Tunneling (SET), Quantum Cellular Automata (QCA), and Tunneling Phase Logic (TPL). Among these, QCA seems to be the most promising emerging technology, as a viable alternative to CMOS. ALU is a fundamental building block of a central processing unit (CPU) in any computing system. Using reversible logic gates instead of traditional logic AND/OR gates, a reversible ALU whose function is the same as traditional ALU is constructed. Programmable reversible logic gates are realized in Verilog HDL, the simulation results have been verified using the QCADesigner. Reversible logic has ability to reduce the power dissipation which is the main requirement in low power digital design. By using the inverse property of reversible logic, all the inputs can be regenerated at the outputs. Thus, by comparing the original inputs with the regenerated inputs, the faults in reversible circuits can be detected. Minimization of the garbage outputs is one of the main goals in reversible logic design and synthesis. The design is based on the reversible multiplexer (RM) synthesized by compact 2:1 QCA multiplexers. The reversible multiplexer is able to achieve 100% fault tolerance in the presence of single missing or additional cell defects in QCA layout. The RALU circuit can be tested for classical unidirectional stuck-at faults using the constant variable used in this design. The experimentation establishes that the proposed RALU outperforms the conventional reversible- ALU's programmability/testability.

Keywords: RTD, SET, TPL, QCA, Verilog HDL, reversible multiplexer (RM), reversible ALU.

I. INTRODUCTION

The International Technology Roadmap for Semiconductors (ITRS) has proposed a few alternative technologies that can replace the transistor based computation in the near future. Some of them are, Resonant Tunneling Diodes (RTD's), Single Electron Tunneling (SET), Quantum Cellular Automata (QCA), Tunneling Phase Logic (TPL), Carbon nano-tubes and Silicon on Insulator (SOI). Among these QCA seems to be the most promising technology that would replace CMOS devices in the near future. Theoretically the idea of cellular automata (CA) was introduced in early 1940s by Von Neumann and Ulam. Later in the year 1993 Lent et al. experimentally demonstrated the possibility of Quantum Dot Cellular Automata cell, with Aluminium Island acting as Quantum dots A quantum dot is a region in the cell structure where charge can localize. A QCA cell consists of _2n' quantum dots with _n' mobile electrons, which can tunnel between the quantum dots of a cell. The compensating positive charge is fixed and immobile. Tunneling out of the cell is completely suppressed due to the potential barriers between the cells. reversibility is the property of circuits in which there is one-to-one mapping between the inputs and the output vectors, that is for each input vector there is a unique output vector and vice-versa. Researchers have proved that each bit of information lost will produce KTln2 Joules of heat energy. The energy dissipated due to information destruction will be a significant factor of the overall heat dissipation of the system. In QCA, computing logic states of 1 and 0 are represented by the position of the electrons inside the QCA cell as illustrated . Thus, when the bit is flipped from 1 to 0 there is no actual discharging of the capacitor as in conventional CMOS. Further, propagation of the polarization from one cell to another is because of interaction of the electrons in adjacent QCA cells. As there is no movement of electrons from one QCA cell to the other, there is no current flow. Thus, QCA has no dissipation in signal propagation. Due to high error rates in nano-scale manufacturing, QCA and other nano-technologies target reducing device error.

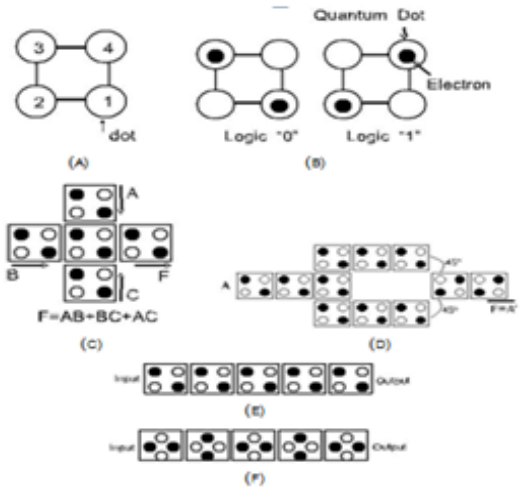

Fig 1: QCA cell and basic QCA Devices. (a) QCA 4 Dots (b) QCA cell as Logic "1"and logic "0", (c)MV,(d) Inverter (INV) , (e) Binary wire, (f) INV chain

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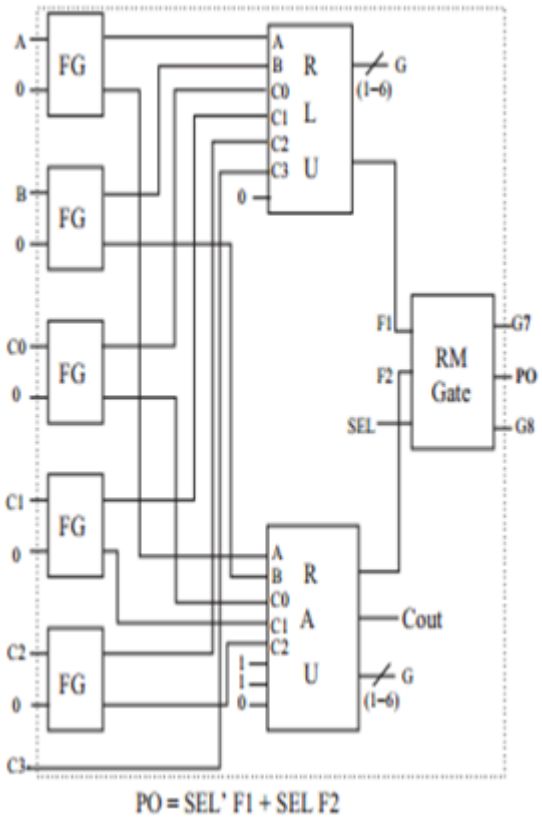
A QCA cell is a coupled dot system in which four dots are at the vertices of a square. The cell has two extra electrons that occupy the diagonals within the cell due to electrostatic repulsion. Fig. 1(a) and (b) shows the four quantum dots in a QCA cell, and the implementation of logic "0" and logic "1" in a QCA cell, respectively. The basic QCA device is the MV or majority gates, which is represented as F = A B + BC + AC , where F is the majority of the inputs A, B, and C. Another important gate in QCA is the INV. There can be many ways of designing the QCA INV, one of which is shown in Fig. 1(d). In QCA computing, signal transfer is made through wires that are of two types: 1) binary wire and 2) INV chain. The binary wire is shown in Fig. 1(e). The INV chain is shown in Fig. 1(f). In QCA, when a binary wire crosses the INV chain, there is no interaction between the two; hence, the signals in the INV chain and binary wire can pass over each other. In QCA computing, the clock helps in the synchronization of circuits and provides the power required for functionality. QCA clocking consists of four phases: switch, hold, release, and relax.

Our proposed work explores the design of a reversible arithmetic and logic unit (RALU) in QCA Technology. The major contributions of this work revolving around logic based QCA architecture can be summarized in the following points:

- Design of a cost-effective 2:1 multiplexer using QCA followed by its cost effective approach toward least chip-area coverage.
- Synthesis of a reversible structure of 2:1 multiplexer (RM) by compact 2:1 multiplexer.
- Design of reversible logic unit (RLU) and arithmetic unit (RAU) using the proposed reversible multiplexer followed by synthesis of the reversible arithmetic and logic unit with the increase in programmability. The proposed design of RALU is shown to be most efficient on the basis of function generation capability and speed of computation.
- Development of the concurrent testing strategy for detection of any stuck-at fault using only two test vectors.

A. ARCHITECTURE OF REVERSIBLE TESTABLE ALU

The arithmetic logic unit (ALU) is an important constituent of the CPU, as it performs most of the arithmetic and logical operations. It has become an utmost necessity for an effective reversible circuit to increase the depth of programmability of the logic device, i.e. the number of logical calculations produced on the fixed outputs. Also, for a flexible ALU, any modification for implementation in an instruction set architecture should be simple. All of the above factors suggest a modular design methodology, as described in the following subsections. Here, reversible ALU (RALU) is synthesized with two separate modules, a reversible logic unit (RLU) and a reversible arithmetic unit (RAU), based on the RM logic gate. An RM gate enables selection of the output from either the RLU or the RAU.



II .CONVENTIONAL METHOD: GATED DIFFUSION INPUT (GDI) TECHNIQUE

Morgenshtein has proposed basic GDI cell shown in figure. For designing of low power digital combinational circuit GDI technique is the new approach. GDI technique is basically two transistor implementation of complex logic functions which provides in-cell swing restoration under certain operating condition. GDI technique approach leads to reduction in propagation delay, area and power consumption of digital circuits is obtained while having low complexity of logic design. In GDI technique the important feature is that the source of the PMOS is not connected to VDD and the source of the NMOS is not connected to GND. Therefore GDI design more flexible than CMOS design.

There are three inputs in a GDI cell - G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of NMOS). Bulks of both NMOS and PMOS are connected to N and P respectively.

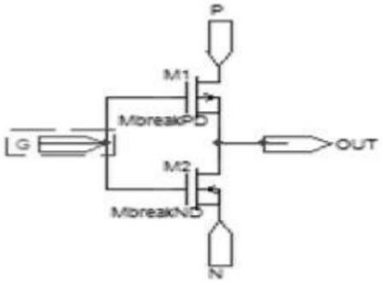


Fig .Basic GDI Cell

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Table shows different logic functions implemented by GDI logic based on different input values. So, various logic functions can be implemented using GDI technique with less power and high speed as compared to conventional CMOS design.

S.NO	N	P	G	Out
1	0	B	A	A'B
2	B	1	A	A'+B
3	1	B	A	A+B
4	B	0	A	AB
5	C	B	A	A'B+AC
6	0	1	A	A'

Fig.GDI Cell Logic Table

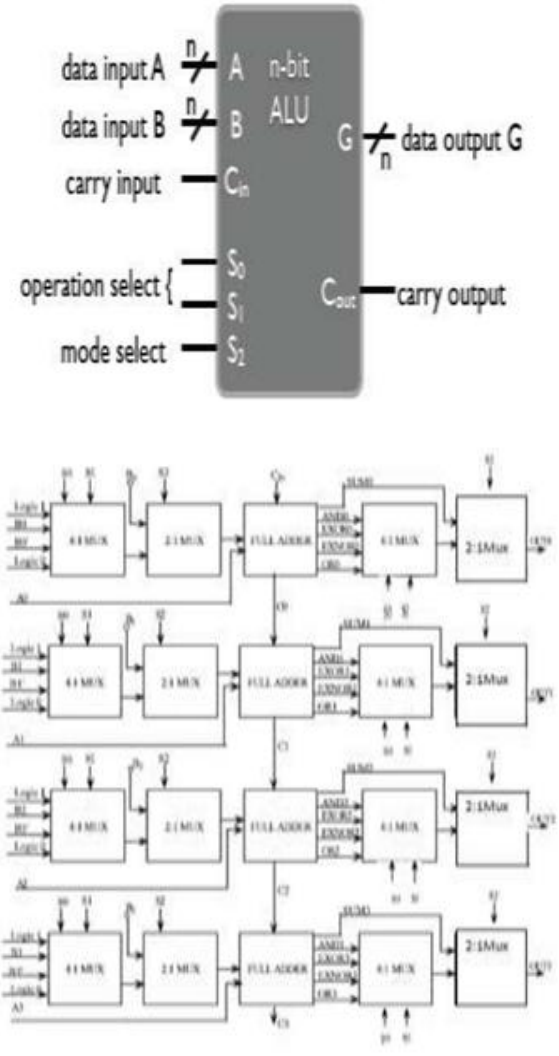

Fig.GDI technique based 4-bit ALU

In Central Processing Unit (CPU) of a computer, Arithmetic and Logic Unit (ALU) is a fundamental building block and even the simplest microprocessors contain ALU. It is responsible for performing arithmetic as well as logical operations such as addition, subtraction, increment ,decrement, logical AND, logical OR, logical XOR and logical XNOR. Eight 4x1 multiplexers, eight 2x1 multiplexers and four full adders are present in 4bit ALU. The 4-bit ALU is designed in 250nm, n-well CMOS technology. An INCREMENT and DECREMENT operations takes place when logic '1'and logic '0' are applied as an input. An INCREMENT operation is analyzed as adding '1' to the addend and DECREMENT is seen as a subtraction operation. For SUBTRACTION operation two's complement method is used in which complement of B is used. The outputs obtained from the full adder are SUM, EXOR, EXNOR, AND & OR.The 4-bit ALU where first stage to fourth stage is cascaded with the CARRY bit. Symbolic representation of 4-bit ALU as shown in figure. Based on the condition of the select signals, the multiplexer selects the appropriate input and gives it to the full adder which then computes the results. At the output of the multiplexer stage selects the appropriate output and route it to output port. Table shows the truth table for the operations performed by the ALU based on the status of the select signal .The operation being performed and the inputs and outputs being selected are determined by set of three select signals incorporated in the design Figure. shows multiplexer logic at input port and Figure. Shows multiplexer logic at output port.

Selection Lines			Operations
S2	S1	S0	
0	0	0	AND
0	0	1	EXOR
0	1	0	EXNOR
0	1	1	OR
1	0	0	ADDITION
1	0	1	SUBSTRACTION
1	1	0	INCREMENT
1	1	1	DECREMENT

2.4.Operations of ALU

By using schematic editor of Tanner EDA the schematic of 4 bit ALU is designed. It shows connectivity between the components and describes aspect ratios of the transistor that can be modified along with the design. Figure represents the complete schematic view of ALU. The 4-bit ALU consists of two 4-bit inputs, three selecting lines, and one carry input, one carry output and four output bits.

III. PROPOSED METHOD

The arithmetic logic unit (ALU) is an important constituent of the CPU, as it performs most of the arithmetic and logical operations. It has become an utmost necessity for an effective reversible circuit to increase the depth of programmability of the logic device, i.e. the number of logical calculations produced on the fixed outputs. Also, for a flexible ALU, any modification for implementation in an instruction set architecture should be

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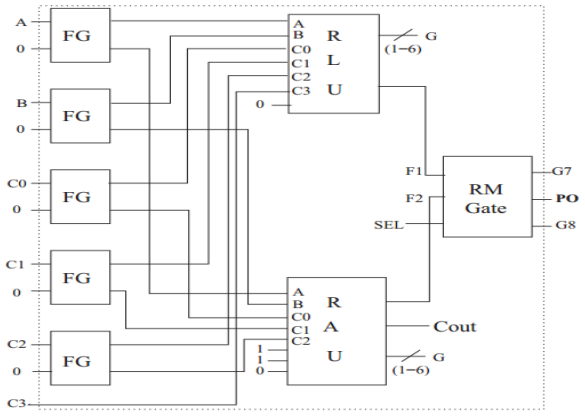

Fig..Block Diagram of Proposed ALU

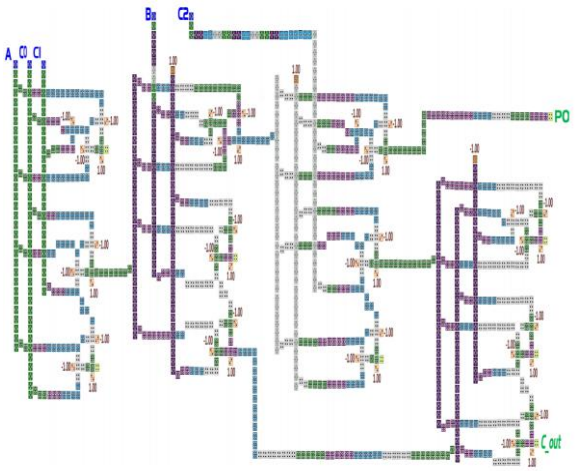

Fig.QCA Design of proposed ALU

Fault test table of reversible arithmetic logic unit.

Input A	Input B	Fault-free output (PO)	Input A Stuck at 0	Input A Stuck at 1	Input B Stuck at 0	Input B Stuck at 1	Both input Stuck at 0	Stuck at A=0, B=1	Stuck at A=1, B=0	Both input Stuck at 1
Reversible logic unit										
0	0	C0	C0	C1	C0	C2	C0	C2	C1	C3
0	1	C2	C2	C3	C0	C2	C0	C2	C1	C3
1	0	C1	C0	C1	C1	C3	C0	C2	C1	C3
1	1	C3	C2	C3	C1	C3	C0	C2	C1	C3
Reversible arithmetic unit										
0	0	X	X	Y	X	X′	X	X′	Y	Y′
0	1	X′	X′	Y′	X	X′	X	X′	Y	Y′
1	0	Y	X	Y	Y	Y′	X	X′	Y	Y′
1	1	Y′	X′	Y′	Y	Y′	X	X′	Y	Y′

Here, X=C0 ⊕C2, Y=C1 ⊕C2.

IV. RESULTS

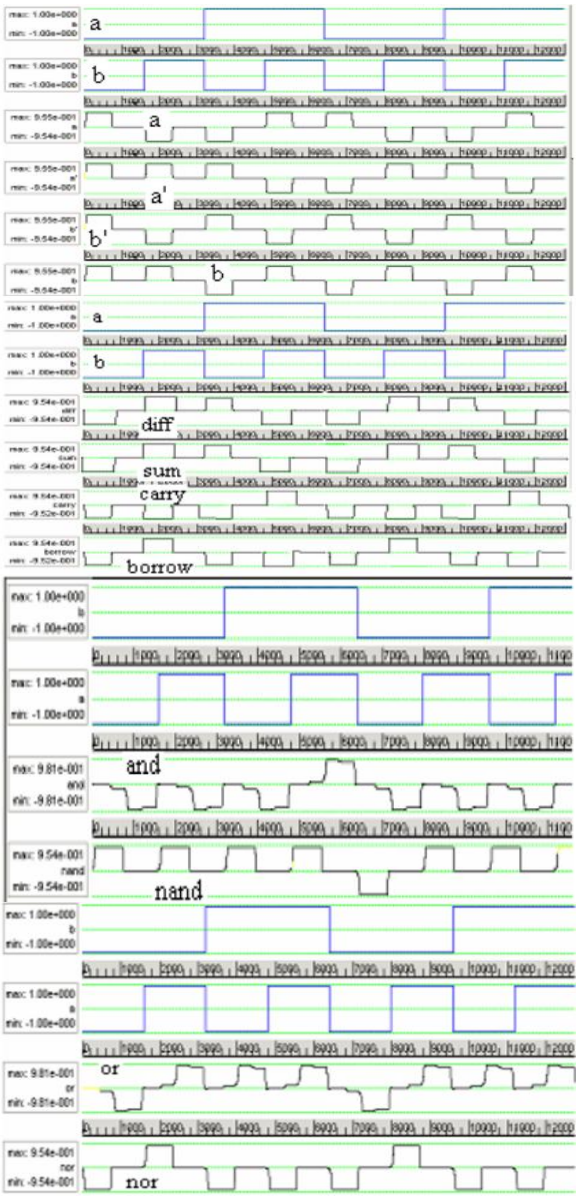

Fig. Simulated wave form QCA ALU

V CONCLUSION

This work proposes a modular reversible arithmetic logic unit (RALU) which consists of two separate modules –

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reversible logic (RLU) and reversible arithmetic unit (RAU). Both the RLU and the RAU are synthesized based on reversible multiplexer (RM) logic introduced in this work having 59% inherent fault tolerance capability in QCA technology. The 100% fault tolerance capability against single missing and additional cell deposition in QCA can be attained by using a fault tolerant structure for few logic primitives inside it. The reversible multiplexer (RM) is synthesized based on three irreversible 2:1 multiplexers proposed in this work. The proposed 2:1 irreversible multiplexer has superiority over the conventional designs available in QCA. The resulting design consists of 19 cells covering an area of only 0.02 μm2, which is substantially lower than the existing ones and uses lesser clock cycles for functioning. The proposed RALU circuits based on reversible multiplexer outperform the ALU circuit implemented with classical gates in terms of testability. The primary advantage of the proposed RALU circuits compared to the conventional ALU circuit is the need of only two test vectors. The decrease in the number of test vectors minimizes the operating expense of test time for a reversible ALU circuit.

REFERENCES

[1] C.S. Lent, P.D. Tougaw, W. Porod, G.H. Bernstein, Quantum cellular automata, Nanotechnology 4 (1993) 49–57.
[2] H. Thapliyal, N. Ranganathan, S. Kotiyal, Design of testable reversible sequential circuits, IEEE Trans. Very Large Scale Integr. Syst. (2012).
[3] A. Chaudhary, D.Z. Chen, X.S. Hu, M.T. Niemier, R. Ravichandran, K. Whitton,Fabricatable interconnect and molecular QCA circuits, IEEE Trans. CAD Integr.Circuits Syst. 26 (2007) 1978–1991.
[4] S.F. Murphy, M. Ottavi, M. Frank, E. DeBenedictis, On the Design of Reversible QDCA Systems, Technical Report, SAND2006-5990, 2006.
[5] J. Ren, V. Semenov, Progress with physically and logically reversible superconducting digital circuits, IEEE Trans. Appl. Supercond. 21 (2011) 780–786.
[6] V.V. Zhirnov, R.K. Cavin, J.A. Hutchby, S. Member, George, I. Bourianoff, Limits to binary logic switch scaling—a Gedanken model, in: Proceedings of the IEEE.
[7] R. Landauer, Irreversibility and heat generation in the computational process,IBM J. Res. Dev. 5 (1961) 183–191. [8] C. Bennett, Logical reversibility of computation. IBM J. Res. Dev. (November) (1973) 525–532.
[9] W. Athas, L. Svensson, J. Koller, N. Tzartzanis, E. Ying-Chin Chou, Low-power digital systems based on adiabatic-switching principles, IEEE Trans. Very Large Scale Integr. Syst. 2 (1994) 398–407.\
[10] C.S. Lent, M. Liu, Y. Lu, Bennett clocking of quantum-dot cellular automata and the limits to binary logic scaling, Nanotech